```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 6
description:
top level BOM
----------------------------
revision 3.932
date: 1995/07/20 01:29:56;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/include

add {,un}stall_all_but_zero routines to end.S
----------------------------
revision 3.931
date: 1995/07/20 01:28:06;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools
      stgen

only let cyl 0 turn on dram and hermes channels
----------------------------
revision 3.930
date: 1995/07/19 06:03:44;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ce

fix bug doublemctest_0
----------------------------
revision 3.929
date: 1995/07/18 22:14:31;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr

drout.V: the tag queue was doing a logical OR of 'write' and 'readdone' to
generate the pop signal. Readdone, actually, is write OR readdone causing the
tag queue to pop twice per write. This got the tags out of order and generally
hosed things. Noticed by a standalone test: long.

drtester.V: the tester was not properly tieing NBprbgrantdr with the clock edge
and with cb2. Changed default test from demo to long.

No placement change.
----------------------------
revision 3.928
date: 1995/07/17 16:13:08;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools/regdepend

forgot to put a "r" in front of register number
----------------------------
revision 3.927
date: 1995/07/16 17:18:31;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

updating top level routing stuff.  No netlist changes
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/doc/Attic/cerberus.mif,v
Working file: doc/cerberus.mif
head: 4.39
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 53;    selected revisions: 1
description:
----------------------------
revision 4.37
date: 1995/07/20 19:10:06;  author: bobm;  state: Exp;  lines: +81 -24
checking in a few recent small changes to prepare for
shared source with cronus.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/euterpe-microarch.book,v
Working file: doc/euterpe-microarch.book
head: 4.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;    selected revisions: 1
description:
----------------------------
revision 4.14
date: 1995/07/20 19:08:11;  author: bobm;  state: Exp;  lines: +3 -2
checking in a few recent small changes to prepare for
shared source with cronus.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/memory.mif,v
Working file: doc/memory.mif
head: 4.36
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 1
description:
----------------------------
revision 4.36
date: 1995/07/20 19:08:42;  author: bobm;  state: Exp;  lines: +231 -69
checking in a few recent small changes to prepare for
shared source with cronus.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/newchanges.mif,v
Working file: doc/newchanges.mif
head: 16.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
```

```
description:
----------------------------
revision 16.13
date: 1995/07/20 19:10:53;  author: bobm;  state: Exp;  lines: +52 -20
checking in a few recent small changes to prepare for
shared source with cronus.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 3
description:
----------------------------
revision 4.201
date: 1995/07/20 01:29:19;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/include

add {,un}stall_all_but_zero routines to end.S
----------------------------
revision 4.200
date: 1995/07/20 01:27:27;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools
      stgen

only let cyl 0 turn on dram and hermes channels
----------------------------
revision 4.199
date: 1995/07/17 16:12:43;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools/regdepend

forgot to put a "r" in front of register number
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/Makefile.defs,v
Working file: verify/Makefile.defs
head: 1.43
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 43;    selected revisions: 1
description:
----------------------------
revision 1.40
date: 1995/07/18 22:53:35;  author: doi;  state: Exp;  lines: +2 -7
get rid of TCC=tgcc override
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/Makerules.local,v
Working file: verify/Makerules.local
head: 3.16
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 3.14
date: 1995/07/18 22:54:10;  author: doi;  state: Exp;  lines: +13 -9
add rule for .cie targets and no longer include verify/Makefile.rules
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/status,v
Working file: verify/status
head: 3.64
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 64;    selected revisions: 2
description:
----------------------------
revision 3.33
date: 1995/07/21 04:01:27;  author: dit00;  state: Exp;  lines: +32 -0
Periodic update
----------------------------
revision 3.32
date: 1995/07/19 15:11:40;  author: dit00;  state: Exp;  lines: +48 -0
Periodic update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/include/BOM,v
Working file: verify/include/BOM
head: 36.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 70;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 35.0
date: 1995/07/20 01:28:53;  author: doi;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/include

add {,un}stall_all_but_zero routines to end.S
----------------------------
revision 34.1
date: 1995/07/20 01:28:35;  author: doi;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/include/end.S,v
Working file: verify/include/end.S
head: 1.38
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 38;    selected revisions: 1
description:
----------------------------
revision 1.35
date: 1995/07/20 01:27:55;  author: doi;  state: Exp;  lines: +43 -1
add {,un}stall_all_but_zero routines to end.S
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 3
description:
----------------------------
revision 1.179
date: 1995/07/20 22:55:28;  author: jeffm;  state: Exp;  lines: +7 -2
Test meltdown type reset.
----------------------------
revision 1.178
date: 1995/07/19 18:22:44;  author: jeffm;  state: Exp;  lines: +2 -2
Hammer a bit on register 1 nb-load use and anti-use for event entry and
exit.
----------------------------
revision 1.177
date: 1995/07/19 00:14:04;  author: jeffm;  state: Exp;  lines: +2 -2
Thrash on cache controller by having all cylinder have cached event
handlers in aliases of the same cache location.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/bgate_perf.S,v
Working file: verify/perf/bgate_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:00:55;  author: claseman;  state: Exp;  lines: +2 -74
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/bgatei_perf.S,v
Working file: verify/perf/bgatei_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:00:58;  author: claseman;  state: Exp;  lines: +2 -74
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/bi_perf.S,v
Working file: verify/perf/bi_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:00:59;  author: claseman;  state: Exp;  lines: +2 -74
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/cable_loop_perf.S,v
Working file: verify/perf/cable_loop_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/17 21:57:07;  author: claseman;  state: Exp;  lines: +53 -76
make sure other cyclinders are idle before stsrting test
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/cerb_perf.S,v
Working file: verify/perf/cerb_perf.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 1.7
date: 1995/07/18 18:01:01;  author: claseman;  state: Exp;  lines: +2 -74
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/dcache_perf.S,v
Working file: verify/perf/dcache_perf.S
head: 1.6
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 1.6
date: 1995/07/18 18:01:03;  author: claseman;  state: Exp;  lines: +1 -68
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/dcachemiss_perf.S,v
Working file: verify/perf/dcachemiss_perf.S
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/07/18 18:01:06;  author: claseman;  state: Exp;  lines: +1 -68
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/dram_perf.S,v
Working file: verify/perf/dram_perf.S
head: 1.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 1.6
date: 1995/07/18 18:01:08;  author: claseman;  state: Exp;  lines: +2 -71
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/eaddi_perf.S,v
Working file: verify/perf/eaddi_perf.S
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 1.2
date: 1995/07/18 18:01:09;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/easum_perf.S,v
```

```
Working file: verify/perf/easum_perf.S
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 1.2
date: 1995/07/18 18:01:11;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/eshufflei4mux_perf.S,v
Working file: verify/perf/eshufflei4mux_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/18 18:01:15;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gcompress16_perf.S,v
Working file: verify/perf/gcompress16_perf.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.3
date: 1995/07/18 18:01:17;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gcompress64_perf.S,v
Working file: verify/perf/gcompress64_perf.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.3
date: 1995/07/18 18:01:19;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gextracti128_perf.S,v
Working file: verify/perf/gextracti128_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/18 18:01:24;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gextracti64_perf.S,v
Working file: verify/perf/gextracti64_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/18 18:01:26;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/ggfmul8_perf.S,v
Working file: verify/perf/ggfmul8_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/18 18:01:29;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gmdepi1_perf.S,v
Working file: verify/perf/gmdepi1_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
```

```
revision 3.2
date: 1995/07/18 18:01:32;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gmdepi64_perf.S,v
Working file: verify/perf/gmdepi64_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:01:35;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd16_perf.S,v
Working file: verify/perf/gmuladd16_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/18 18:01:38;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd32_perf.S,v
Working file: verify/perf/gmuladd32_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/18 18:01:42;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd64_perf.S,v
Working file: verify/perf/gmuladd64_perf.S
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/07/18 18:01:46;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd8_perf.S,v
Working file: verify/perf/gmuladd8_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/18 18:01:56;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gselect8_perf.S,v
Working file: verify/perf/gselect8_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:01:58;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gsete64_perf.S,v
Working file: verify/perf/gsete64_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:02:01;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gtranspose8mux_perf.S,v
Working file: verify/perf/gtranspose8mux_perf.S
head: 3.2
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:02:04;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/hermes_perf.S,v
Working file: verify/perf/hermes_perf.S
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/07/18 18:02:06;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/icachemiss_perf.S,v
Working file: verify/perf/icachemiss_perf.S
head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/07/18 18:02:09;  author: claseman;  state: Exp;  lines: +1 -70
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/lu32li_perf.S,v
Working file: verify/perf/lu32li_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:02:12;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/lu8i_perf.S,v
```

```
Working file: verify/perf/lu8i_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:02:14;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/mbnez_perf.S,v
Working file: verify/perf/mbnez_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:02:15;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/rom_perf.S,v
Working file: verify/perf/rom_perf.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 1.7
date: 1995/07/18 18:02:17;  author: claseman;  state: Exp;  lines: +2 -72
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/saas64la_perf.S,v
Working file: verify/perf/saas64la_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:02:19;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/smas64la_perf.S,v
Working file: verify/perf/smas64la_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/18 18:02:22;  author: claseman;  state: Exp;  lines: +2 -73
use global print routine
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1122.S,v
Working file: verify/random/regdepend_r1122.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:48:55;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1639.S,v
Working file: verify/random/regdepend_r1639.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:48:58;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1847.S,v
Working file: verify/random/regdepend_r1847.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
```

```
revision 3.2
date: 1995/07/19 22:49:01;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2075.S,v
Working file: verify/random/regdepend_r2075.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/07/19 22:49:18;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2279.S,v
Working file: verify/random/regdepend_r2279.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:49:04;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2476.S,v
Working file: verify/random/regdepend_r2476.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:49:08;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2493.S,v
Working file: verify/random/regdepend_r2493.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:49:21;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2688.S,v
Working file: verify/random/regdepend_r2688.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:49:12;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r3362.S,v
Working file: verify/random/regdepend_r3362.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:49:15;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5557.S,v
Working file: verify/random/regdepend_r5557.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:49:25;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5757.S,v
Working file: verify/random/regdepend_r5757.S
head: 3.2
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:49:28;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5957.S,v
Working file: verify/random/regdepend_r5957.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:49:31;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6968.S,v
Working file: verify/random/regdepend_r6968.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 4.2
date: 1995/07/19 22:49:34;  author: dit00;  state: Exp;  lines: +1 -1
Add magic fix
----------------------------
revision 4.1
date: 1995/07/17 03:57:31;  author: dit00;  state: Exp;
Add new test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7168.S,v
Working file: verify/random/regdepend_r7168.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 4.2
date: 1995/07/19 22:49:37;  author: dit00;  state: Exp;  lines: +1 -1
```

```
Add magic fix
----------------------------
revision 4.1
date: 1995/07/17 03:57:34;  author: dit00;  state: Exp;
Add new test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7363.S,v
Working file: verify/random/regdepend_r7363.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 4.2
date: 1995/07/19 22:49:41;  author: dit00;  state: Exp;  lines: +1 -1
Add magic fix
----------------------------
revision 4.1
date: 1995/07/17 03:57:37;  author: dit00;  state: Exp;
Add new test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r754.S,v
Working file: verify/random/regdepend_r754.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/19 22:48:51;  author: dit00;  state: Exp;  lines: +4 -0
Add magic fix
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7563.S,v
Working file: verify/random/regdepend_r7563.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/16 00:51:27;  author: dit00;  state: Exp;
Add new test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r8162.S,v
```

```
Working file: verify/random/regdepend_r8162.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 4.2
date: 1995/07/19 22:49:45;  author: dit00;  state: Exp;  lines: +1 -1
Add magic fix
----------------------------
revision 4.1
date: 1995/07/16 19:52:25;  author: dit00;  state: Exp;
Add new test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/status,v
Working file: verify/random/status
head: 2.26
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 3
description:
----------------------------
revision 2.17
date: 1995/07/19 16:02:20;  author: dit00;  state: Exp;  lines: +2 -0
Perodic update
----------------------------
revision 2.16
date: 1995/07/17 21:43:22;  author: dit00;  state: Exp;  lines: +6 -1
Periodic update
----------------------------
revision 2.15
date: 1995/07/16 01:06:13;  author: dit00;  state: Exp;  lines: +4 -0
Periodic update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r11725.S,v
Working file: verify/random/stgen_r11725.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/15 23:24:17;  author: dit00;  state: Exp;
Add new test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/template,v
```

```
Working file: verify/random/template
head: 2.33
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 33;    selected revisions: 3
description:
----------------------------
revision 2.21
date: 1995/07/19 16:02:25;  author: dit00;  state: Exp;  lines: +1 -1
Perodic update
----------------------------
revision 2.20
date: 1995/07/17 21:43:25;  author: dit00;  state: Exp;  lines: +7 -7
Periodic update
----------------------------
revision 2.19
date: 1995/07/16 01:06:17;  author: dit00;  state: Exp;  lines: +10 -10
Periodic update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/BOM,v
Working file: verify/tools/BOM
head: 13.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 90;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 10.2
date: 1995/07/20 01:27:05;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools
      stgen

only let cyl 0 turn on dram and hermes channels
----------------------------
revision 10.1
date: 1995/07/17 16:12:31;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools/regdepend

forgot to put a "r" in front of register number
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/stgen,v
Working file: verify/tools/stgen
head: 5.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
```

```
revision 5.11
date: 1995/07/20 01:26:18;  author: doi;  state: Exp;  lines: +16 -1
only let cyl 0 turn on dram and hermes channels
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/regdepend/BOM,v
Working file: verify/tools/regdepend/BOM
head: 26.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 50;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 26.0
date: 1995/07/17 16:12:17;  author: doi;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/tools/regdepend

forgot to put a "r" in front of register number
----------------------------
revision 25.1
date: 1995/07/17 16:12:10;  author: doi;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/regdepend/regdepend.c,v
Working file: verify/tools/regdepend/regdepend.c
head: 1.29
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 29;    selected revisions: 1
description:
----------------------------
revision 1.29
date: 1995/07/17 16:11:37;  author: doi;  state: Exp;  lines: +2 -2
forgot to put a "r" in front of register number
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185;   selected revisions: 3
description:
----------------------------
revision 1.179
date: 1995/07/20 22:55:28;  author: jeffm;  state: Exp;  lines: +7 -2
Test meltdown type reset.
----------------------------
revision 1.178
```

```
date: 1995/07/19 18:22:44;  author: jeffm;  state: Exp;  lines: +2 -2
Hammer a bit on register 1 nb-load use and anti-use for event entry and
exit.
----------------------------
revision 1.177
date: 1995/07/19 00:14:04;  author: jeffm;  state: Exp;  lines: +2 -2
Thrash on cache controller by having all cylinder have cached event
handlers in aliases of the same cache location.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/dr_debug.sig,v
Working file: verify/toplevel/dr_debug.sig
head: 39.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 39.3
date: 1995/07/18 16:45:58;  author: jeffm;  state: Exp;  lines: +12 -1
Add debug signals.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/exhancacheharder.S,v
Working file: verify/toplevel/exhancacheharder.S
head: 41.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 41.2
date: 1995/07/19 20:54:39;  author: jeffm;  state: Exp;  lines: +2 -2
Fixed so that _V version will assemble.
----------------------------
revision 41.1
date: 1995/07/19 00:13:59;  author: jeffm;  state: Exp;
Thrash on cache controller by having all cylinder have cached event
handlers in aliases of the same cache location.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/exr1harder.S,v
Working file: verify/toplevel/exr1harder.S
head: 41.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 41.2
date: 1995/07/20 22:41:52;  author: jeffm;  state: Exp;  lines: +3 -3
```

```
Change max and min timer values - terp is more accurate now, and
caught that the test wasn't waiting long enough.
----------------------------
revision 41.1
date: 1995/07/19 18:22:41;  author: jeffm;  state: Exp;
Hammer a bit on register 1 nb-load use and anti-use for event entry and
exit.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/meltdowntest.S,v
Working file: verify/toplevel/meltdowntest.S
head: 41.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 41.1
date: 1995/07/20 22:55:21;  author: jeffm;  state: Exp;
Test meltdown type reset.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/meltdowntest.sen,v
Working file: verify/toplevel/meltdowntest.sen
head: 41.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 41.1
date: 1995/07/20 22:55:24;  author: jeffm;  state: Exp;
Test meltdown type reset.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 1
description:
----------------------------
revision 1.125
date: 1995/07/21 03:58:53;  author: dit00;  state: Exp;  lines: +8 -8
Perodic update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;  selected revisions: 3
description:
top level verilog BOM
----------------------------
revision 4.9
date: 1995/07/19 06:03:24;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ce

fix bug doublemctest_0
----------------------------
revision 4.8
date: 1995/07/18 22:14:05;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr

drout.V: the tag queue was doing a logical OR of 'write' and 'readdone' to
generate the pop signal. Readdone, actually, is write OR readdone causing the
tag queue to pop twice per write. This got the tags out of order and generally
hosed things. Noticed by a standalone test: long.

drtester.V: the tester was not properly tieing NBprbgrantdr with the clock edge
and with cb2. Changed default test from demo to long.

No placement change.
----------------------------
revision 4.7
date: 1995/07/16 17:18:13;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

updating top level routing stuff.  No netlist changes
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 4
description:
----------------------------
revision 335.2
date: 1995/07/19 06:03:06;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ce

fix bug doublemctest_0
----------------------------
revision 335.1
date: 1995/07/18 22:13:40;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr

drout.V: the tag queue was doing a logical OR of 'write' and 'readdone' to
generate the pop signal. Readdone, actually, is write OR readdone causing the
```

```
tag queue to pop twice per write. This got the tags out of order and generally
hosed things. Noticed by a standalone test: long.

drtester.V: the tester was not properly tieing NBprbgrantdr with the clock edge
and with cb2. Changed default test from demo to long.

No placement change.
----------------------------
revision 335.0
date: 1995/07/16 17:17:55;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

updating top level routing stuff.  No netlist changes
----------------------------
revision 334.1
date: 1995/07/16 17:17:42;  author: tbr;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.netcap,v
Working file: verilog/bsrc/chip_euterpe-base.netcap
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 4
description:
----------------------------
revision 312.15
date: 1995/07/20 18:13:25;  author: tbr;  state: Exp;  lines: +36672 -36672
another top level iteration
----------------------------
revision 312.14
date: 1995/07/19 20:34:54;  author: tbr;  state: Exp;  lines: +38142 -38149
updated from an iteration
----------------------------
revision 312.13
date: 1995/07/19 05:47:05;  author: tbr;  state: Exp;  lines: +47976 -49178
top level after one iteration powering up and down
----------------------------
revision 312.12
date: 1995/07/16 17:06:36;  author: tbr;  state: Exp;  lines: +5750 -5624
updated for dr fix and rg placement change
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.nof,v
Working file: verilog/bsrc/chip_euterpe-base.nof
head: 307.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 307.11
```

```
date: 1995/07/19 20:14:26;  author: tbr;  state: Exp;  lines: +87016 -87044
updated from an iteration
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.pim,v
Working file: verilog/bsrc/chip_euterpe-base.pim
head: 312.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 3
description:
----------------------------
revision 312.15
date: 1995/07/20 18:05:58;  author: tbr;  state: Exp;  lines: +3 -3
another top level iteration
----------------------------
revision 312.14
date: 1995/07/19 05:50:47;  author: tbr;  state: Exp;  lines: +2 -2
top level after one iteration powering up and down
----------------------------
revision 312.13
date: 1995/07/16 17:01:40;  author: tbr;  state: Exp;  lines: +300 -266
updated for dr fix and rg placement change
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.strength,v
Working file: verilog/bsrc/chip_euterpe-base.strength
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 4
description:
----------------------------
revision 312.15
date: 1995/07/20 18:24:41;  author: tbr;  state: Exp;  lines: +459 -458
another top level iteration
----------------------------
revision 312.14
date: 1995/07/19 20:26:25;  author: tbr;  state: Exp;  lines: +1445 -1445
updated from an iteration
----------------------------
revision 312.13
date: 1995/07/19 05:52:27;  author: tbr;  state: Exp;  lines: +8516 -8532
top level after one iteration powering up and down
----------------------------
revision 312.12
date: 1995/07/16 17:11:06;  author: tbr;  state: Exp;  lines: +2530 -2526
updated for dr fix and rg placement change
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.xrf,v
Working file: verilog/bsrc/chip_euterpe-base.xrf
head: 307.11
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 307.11
date: 1995/07/19 20:23:09;  author: tbr;  state: Exp;  lines: +0 -62770
updated from an iteration
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/BOM,v
Working file: verilog/bsrc/ce/BOM
head: 86.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 170;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 85.0
date: 1995/07/19 06:02:45;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/ce

fix bug doublemctest_0
----------------------------
revision 84.1
date: 1995/07/19 06:02:38;  author: tbr;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cemaster.V,v
Working file: verilog/bsrc/ce/cemaster.V
head: 1.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17;    selected revisions: 1
description:
----------------------------
revision 1.14
date: 1995/07/18 00:20:44;  author: dickson;  state: Exp;  lines: +5 -3
fix bug doublemctest_0. a nand4 was added so placement update
needed. sticky flag upstream of edge detector that starts
reset sequence.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.V,v
Working file: verilog/bsrc/ce/cerberus.V
head: 1.63
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 63;    selected revisions: 1
description:
----------------------------
revision 1.57
date: 1995/07/18 00:20:47;  author: dickson;  state: Exp;  lines: +3 -3
fix bug doublemctest_0. a nand4 was added so placement update
needed. sticky flag upstream of edge detector that starts
reset sequence.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.cpif,v
Working file: verilog/bsrc/ce/cerberus.cpif
head: 1.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 1
description:
----------------------------
revision 1.30
date: 1995/07/18 18:01:45;  author: vo;  state: Exp;  lines: +3 -1
added placement for master/to01
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/BOM,v
Working file: verilog/bsrc/dr/BOM
head: 77.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 155;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 77.0
date: 1995/07/18 22:13:14;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/dr

drout.V: the tag queue was doing a logical OR of 'write' and 'readdone' to
generate the pop signal. Readdone, actually, is write OR readdone causing the
tag queue to pop twice per write. This got the tags out of order and generally
hosed things. Noticed by a standalone test: long.

drtester.V: the tester was not properly tieing NBprbgrantdr with the clock edge
and with cb2. Changed default test from demo to long.

No placement change.
----------------------------
revision 76.1
date: 1995/07/18 22:13:04;  author: woody;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/drout.V,v
```

```
Working file: verilog/bsrc/dr/drout.V
head: 3.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17;    selected revisions: 1
description:
----------------------------
revision 3.17
date: 1995/07/18 21:02:51;  author: woody;  state: Exp;  lines: +4 -2
drout.V: the tag queue was doing a logical OR of 'write' and 'readdone' to
generate the pop signal. Readdone, actually, is write OR readdone causing the
tag queue to pop twice per write. This got the tags out of order and generally
hosed things. Noticed by a standalone test: long.

drtester.V: the tester was not properly tieing NBprbgrantdr with the clock edge
and with cb2. Changed default test from demo to long.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/drtester.V,v
Working file: verilog/bsrc/dr/drtester.V
head: 1.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 21;    selected revisions: 1
description:
----------------------------
revision 1.18
date: 1995/07/18 21:02:53;  author: woody;  state: Exp;  lines: +9 -4
drout.V: the tag queue was doing a logical OR of 'write' and 'readdone' to
generate the pop signal. Readdone, actually, is write OR readdone causing the
tag queue to pop twice per write. This got the tags out of order and generally
hosed things. Noticed by a standalone test: long.

drtester.V: the tester was not properly tieing NBprbgrantdr with the clock edge
and with cb2. Changed default test from demo to long.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v
Working file: verilog/bsrc/rg/BOM
head: 136.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 297;   selected revisions: 2
description:
----------------------------
revision 136.0
date: 1995/07/16 17:16:13;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

updating top level routing stuff.  No netlist changes
----------------------------
```

```
revision 135.1
date: 1995/07/16 17:16:05;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================
```